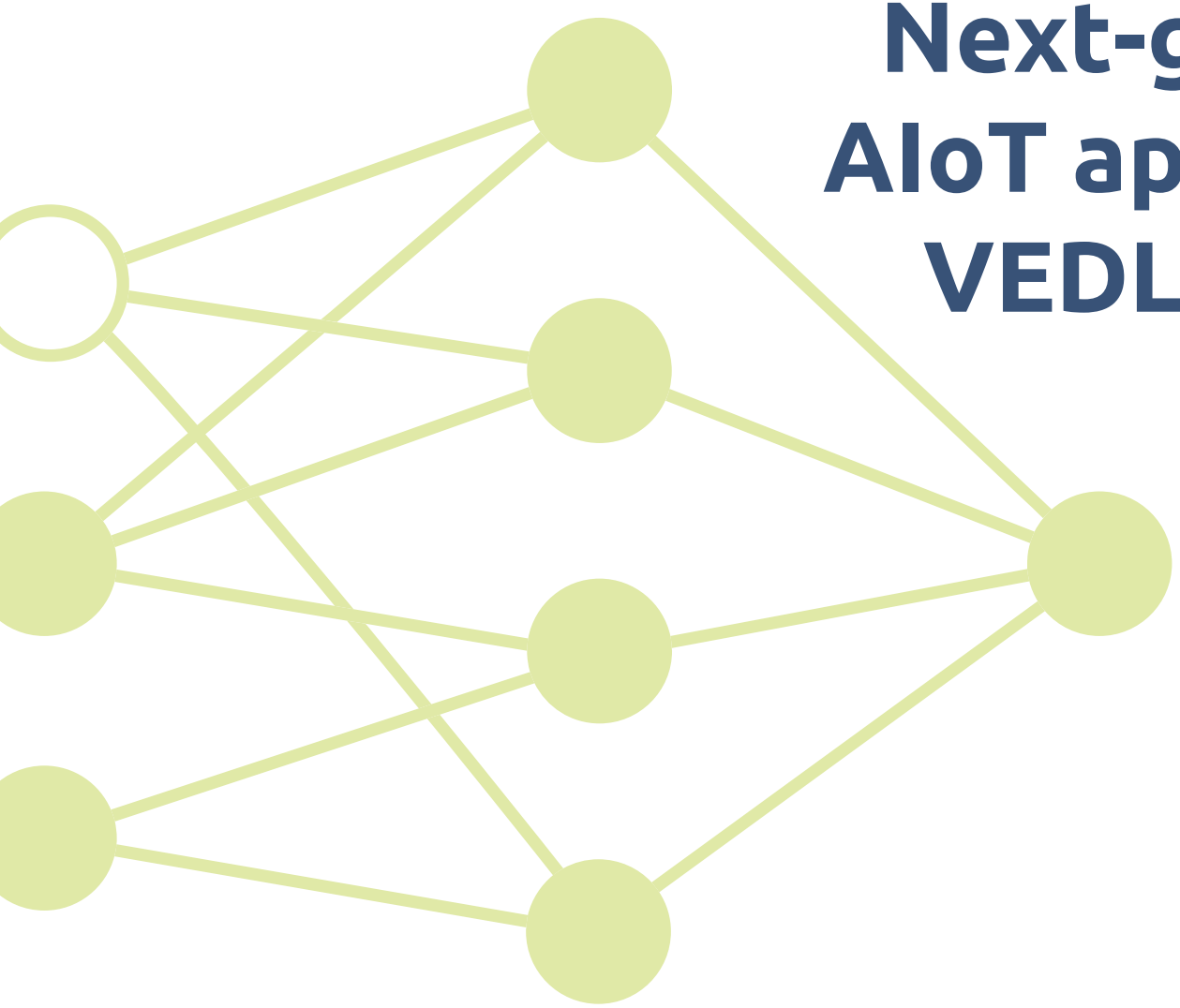
VEDLIoT
Very Efficient Deep Learning in IoT



Next-generation AIoT applications – VEDLIoT-Open

OPEN CALL

The VEDLIoT project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 957197

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Very Efficient Deep Learning for IoT – VEDLIoT

VEDLIoT
Very Efficient Deep Learning in IoT

- **Platform**
  - Hardware: Scalable, heterogeneous, distributed
  - Accelerators: Efficiency boost by FPGA and ASIC technology
  - Toolchain: Optimizing Deep Learning for IoT
- **Use cases**
  - Industrial IoT
  - Automotive
  - Smart Home
- **Open call**
  - At project mid-term
  - Early use and evaluation of VEDLIoT technology

- **Call:** H2020-ICT2020-1
- **Topic:** ICT-56-2020 Next Generation Internet of Things
- **Duration:** 1. November 2020 – 31. Oktober 2023
- **Coordinator:** Bielefeld University (Germany)
- **Overall budget:** 7 996 646.25 €
- **Consortium:** 12 partners from 4 EU countries (Germany, Poland, Portugal and Sweden) and one associated country (Switzerland).

More info:

⇒ https://www.vedliot.eu/
⇒ https://twitter.com/VEDLIoT
⇒ https://www.linkedin.com/company/vedliot/

Next-generation AIoT applications – VEDLIoT-Open

Task: Boost your AIoT application with VEDLIoT technology. Deploy, test, and validate VEDLIoT technology to strengthen your AIoT application in areas such as wearables, transportation, agriculture, homes, health, energy, and manufacturing.

Timeline (targets):

- Submission window: 01.03.-08.05.2022
- Grant signature: First week of July 2022
- Project Start: After Grant signature, latest beginning of August 2022
- Duration: 9 – 12 Months
- Projects need to end June 2023 to be aligned with the overall VEDLIoT project

Indicative budget per project: up to 120,000 € (including 25 % indirect costs, at a funding/reimbursement rate of 70 %)

Indicative budget for the call: up to 840.000 € (~10 projects)

What type of projects are we looking for?

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Proposals should be focused on next generation of IoT applications in areas such as **automation, manufacturing, transportation, automotive, wearables, , agriculture, homes, health, or energy.**

Applicants can be **single participants** or **small consortiums of any size or type** (legal persons, e.g., Universities, Research Institutes, SMEs, startups, or bigger companies).

Specific technology challenges related with one or more of the following application domains should be addressed:

- **Machine learning**
- **Artificial Intelligence of Things**
- **Hardware acceleration**
- **Heterogeneous computing**
- **Near and far edge computing**
- **Reconfigurable computing and run-time reconfiguration**
- **Energy and Resource-efficient system architectures**
- **Security and Privacy for IoT and Edge computing**
- **Federated learning**

Budget:
Indicative budget per project: 120.000 €
- Incl. 25% overhead / indirect costs
- 70% funding / reimbursement rate

Example:
- 96.000 € calculated direct eligible costs
- 120.000 € total budget incl. 24.000 € overhead
- 84.000 € contribution from VEDLIoT-Open (70 % funding)

Application process

Application documents:

Proposal template – PDF / Word
Guide for applicants – PDF

Format: Up to 15 evaluable pages (less is more), Arial, Size 10

Support: vedliot-open-support@vedliot.eu

Submission: One pdf file (< 10 MByte) to

vedliot-open-submission@vedliot.eu

until the 8th of May 2022 at 23:59 CEST, you will receive a direct confirmation. If you want to refine your proposal, simple answer to the confirmation mail (also multiple times).

Evaluation criteria

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Proposals are evaluated based on

- Excellence (Ambition, Concept, Approach)
- Impact (Direct and indirect impact)
- Implementation (Team and ressources)

Each criteria is scored independently from 0 to 5. Individual threshold is 3, while overall threshold is 10, maximum score is 15.

Apart from the overall fit to the application domain, proposals should address their fit to the overall VEDLIoT project, e.g.

- Which VEDLIoT technology will be used
- Benefits for your proposal used VEDLIoT technology and potential VEDLIoT benefit

What‘s in for selected applicants

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Financial support: 70 % of your total project costs

Early access to VEDLIoT technology for your project:

- Project results, i.e., deliverables
- VEDLIoT hardware platform, remote (project testbed) or on-site (hardware loan)
- VEDLIoT toolchain, especially tools like Renode and Kenning (Antmicro)
- VEDLIoT use-cases, possible inspiration/reuse for your project

Support from the VEDLIoT consortium (VEDLIoT-Open mentors):

- One VEDLIoT mentor per project as interface to the main project
- Expert knowledge in areas such as
    - Hardware Accelerators, heterogenous hardware and benchmarks
    - ML/DL models, networks and toolchains
    - Security, safety and requirements engineering for ML systems
    - VELDIoT use cases

IP, Reporting and Payment

- For the duration of the project, VEDLIoT-Open projects will be associated to the main VEDLIoT project:
  - Easy access to VEDLIoT technology and IP required to implement your project
  - VEDLIoT has access to your results as well
  - Participants retain full and exclusive ownership of their IP developed before and during the project. Ownership of any IP developed in collaboration with other parties is shared between the respective parties
- After completion of the project, a final project report has to be submitted, and a presentation of the project needs to be given to the VEDLIoT consortium
- Payment
  - After signing the contract, participant may receive a pre-financing of 40 % of the total amount
  - Final payment will be made at the end of the project after successfully completing the activity and delivering the final report
  - If required, a proposal may define additional payments during the project by including payment milestones coupled with additional deliverables

VEDLIoT Big Picture

VEDLIoT
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Requirements

Smart Home

Industrial IoT

Automotive AI

Security & Safety

Modelling & Verification

Applications

Open Call

Trusted Execution & Communication

Middleware

Optimizer

embedl

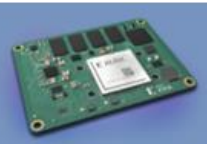
Emulation

RENODE

Benchmarking & Deployment

Kenning

Microserver & Accelerators

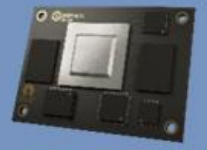


Xilinx Kria

Coral SoM

COM-HPC Xilinx Zynq UltraScale+

Jetson AGX NVIDIA Xavier



RPi CM4 ARVSOM

SMARC Xilinx Zynq UltraScale

Monitoring

Safety & Robustness

Hardware Platforms

Embedded/ Far Edge

uRECS

Near Edge

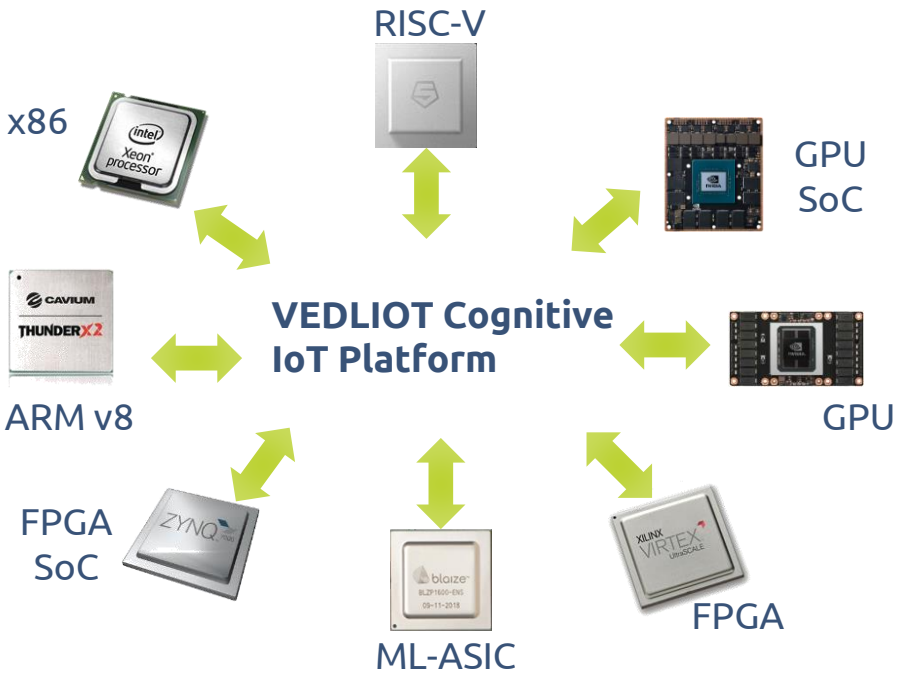
t.RECS

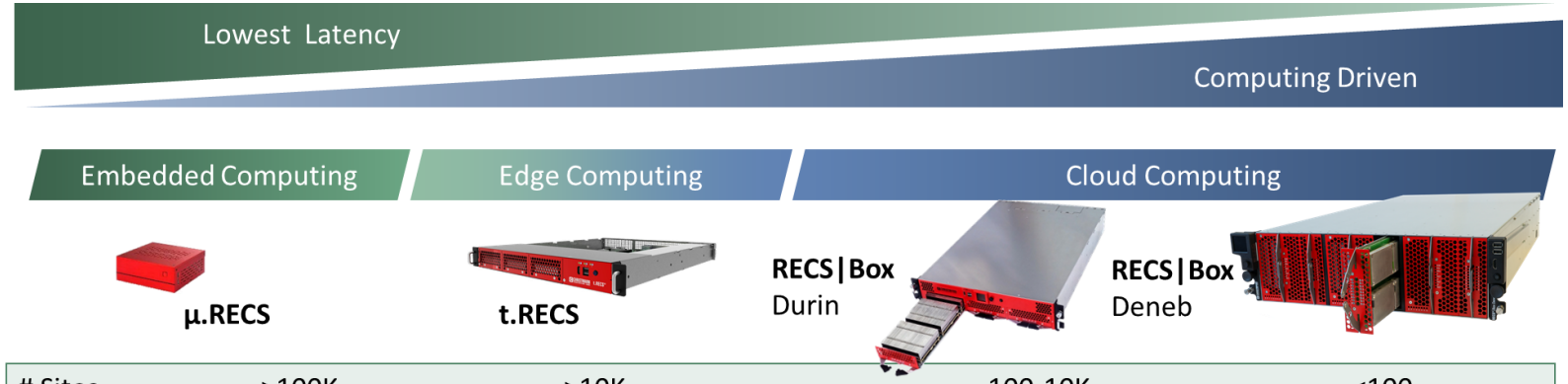
Cloud

RECS|Box

RISC-V extensions

VEDLIoT Hardware Platform





# Sites	>100K	>10K	100-10K	<100
Footprint	Custom	Compact (1RU)	Medium (2RU)	Large (3RU)
Power Budget	<10 W	< 500 W	500 W – 2 KW	> 2 KW
# Microserver	max 2	up to 3	up to 48	up to 144

- Heterogeneous, modular, scalable microserver system
- Supporting the full spectrum of IoT **from embedded over the edge towards the cloud**
- Different technology concepts for improving
  - Performance
  - Cost-effectiveness
  - Maintainability
  - Reliability
  - Energy-Efficiency
  - Safety

RECS Architecture (RECS|BOX)

RECS|BOX

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High-Performance Carrier
(up to 3 microservers)

Low-Power Carrier
(up to 16 microservers)

High-Performance Microserver (COM Express)

x86

ARM v8

FPGA SoC

Low-Power Microserver (Apalis/Jetson)

FPGA SoC

ARM Soc

GPU SoC

RECS Server Backplane (up to 15 Carriers)

Carrier (High Performance)

Microserver (High Performance) #1 #2 #3

Carrier (Low Power)

Microserver (Low Power) #1 #2 #3 ... **Microserver** (Low Power) #16

Carrier (PCIe Expansion)

e.g. GPU-Accelerator

Compute Network (up to 40 GbE)

Management Network (KVM, Monitoring, …)

High-Speed Low-Latency Network (PCIe, High-Speed Serial)

Ext. Connectors

- QSFP+
- HDMI/USB
- RJ45
- iPass+ HD

RECS Architecture (t.RECS)

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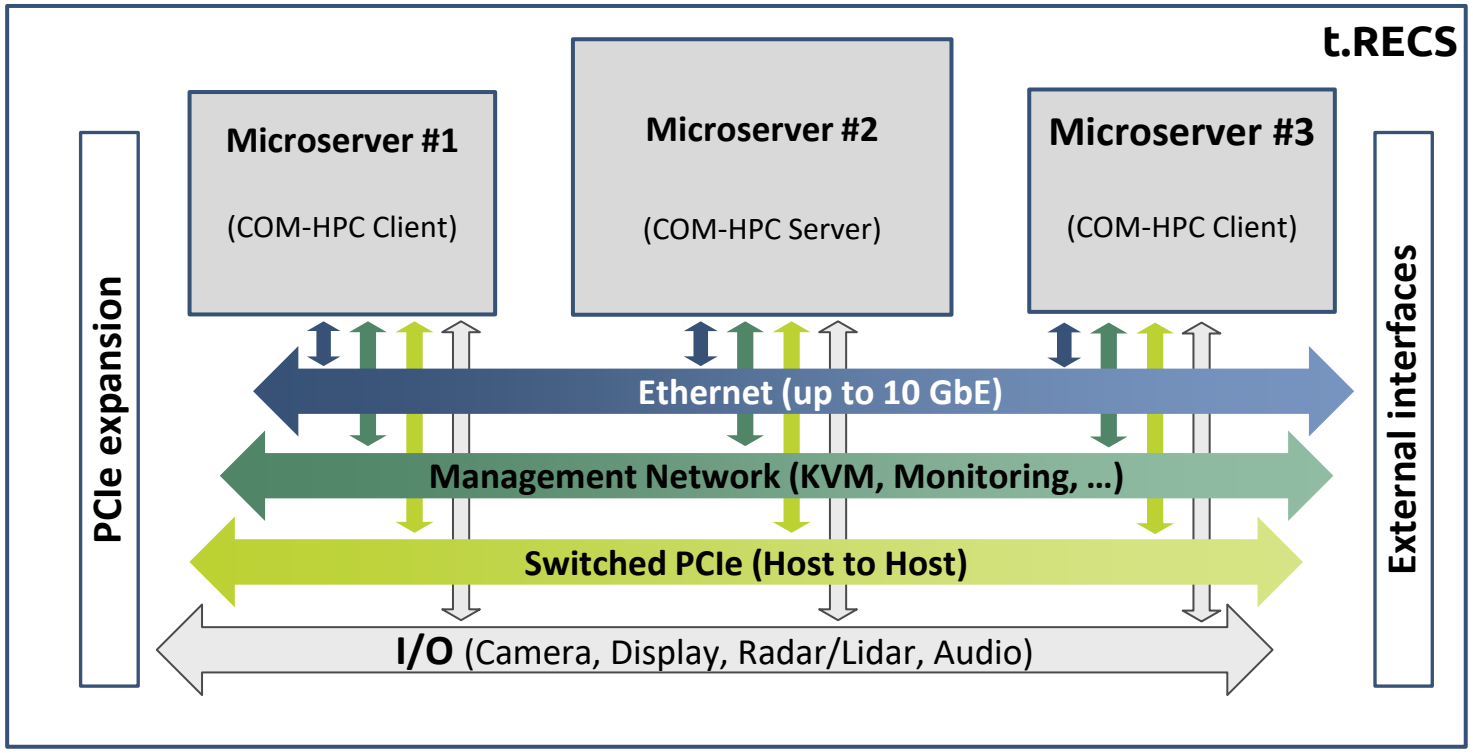
t.RECS Edge Server

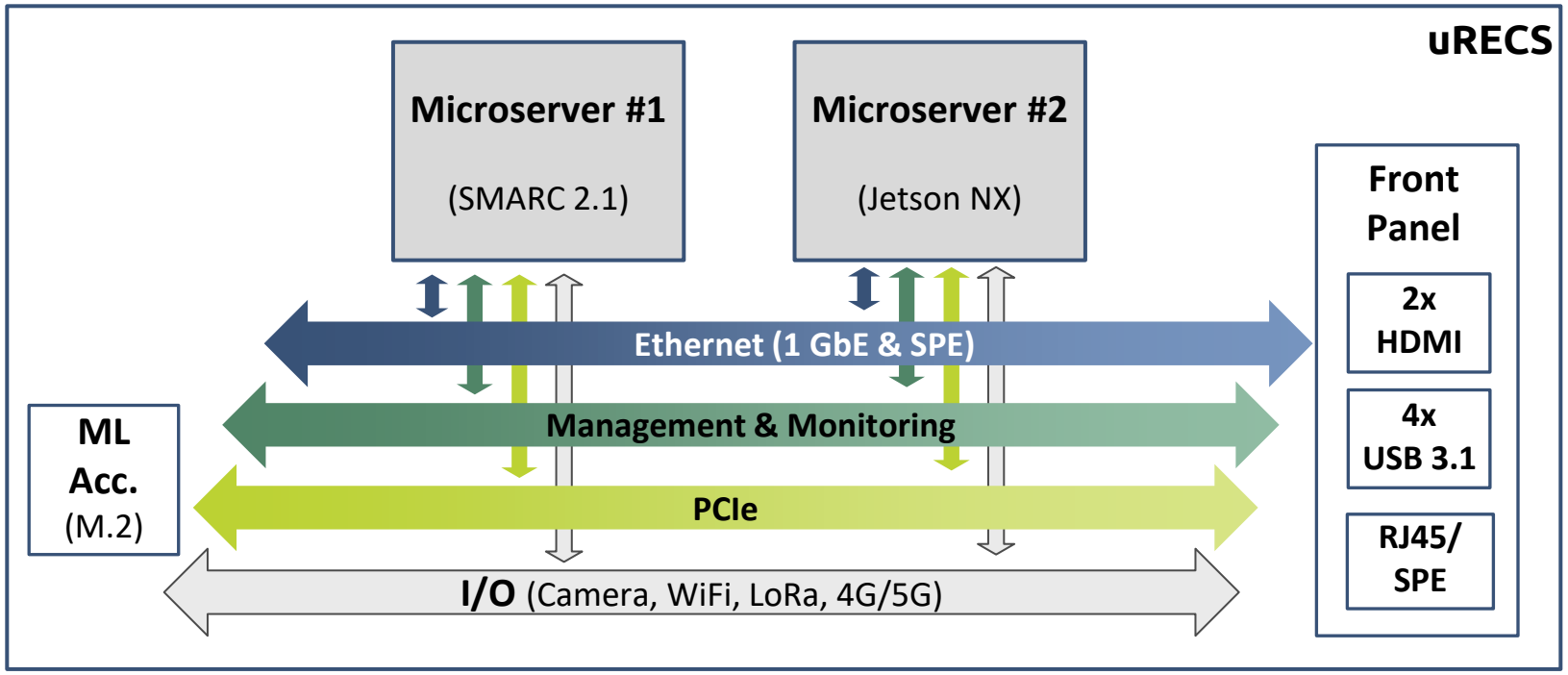
- Optimized platform for local / edge applications
- Provide interfaces for
  - Video
  - Camera
  - Peripheral input (USB)
- Combine FPGA and GPU acceleration
- Compact dimensions
  1 RU, E-ATX form factor
  (2 RU/ 3 RU for special cases)



RECS Architecture (uRECS)

uRECS AIoT Server

- Supports ML acceleration
  - FPGA
  - ASIC
- Communication interfaces
  - Wired (CAN, Ethernet, CSI)
  - Wireless (WLAN, LoRa, 5G)
- Sensors
  - Camera
  - Environment (Temp./Hum.)
  - Housekeeping
- Embedded Device
  (~ 20x20x6 cm)



Microserver overview

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RECS|Box

t.RECS

uRECS

CPU

COM Express
Intel Core i7
8th Gen

Apalis
Exynos (2xARM
Cortex-A15)

COM Express
ARM v8 Server SoC
Hi1616

COM Express
AMD EPYC
3451

COM Express
AMD Ryzen
V1807B

COM-HPC
client size A
Intel Core i7
11th Gen

FPGA SoC

COM Express
Xilinx
Zynq
7045

Apalis
Xilinx Zynq 7020

COM Express
Intel Stratix 10

COM-HPC
client size B
Xilinx Zynq
UltraScale+

COM-HPC
server size D
Intel Agilex

COM-HPC
client size B
Xilinx Versal

GPU SoC

Jetson TX2
NVIDIA
Tegra X2

Jetson nano
NVIDIA
Xavier NX

Jetson AGX
NVIDIA Xavier

COM-HPC Size B
NVIDIA Xavier
AGX

ML SoC

SMARC
Coherent
Logix
HX40416

SMARC
Coral SoM

SMARC
Xilinx Zynq
UltraScale

VEDLIoT Deep Learning Plattforms
Supported Computer-On-Module form factors

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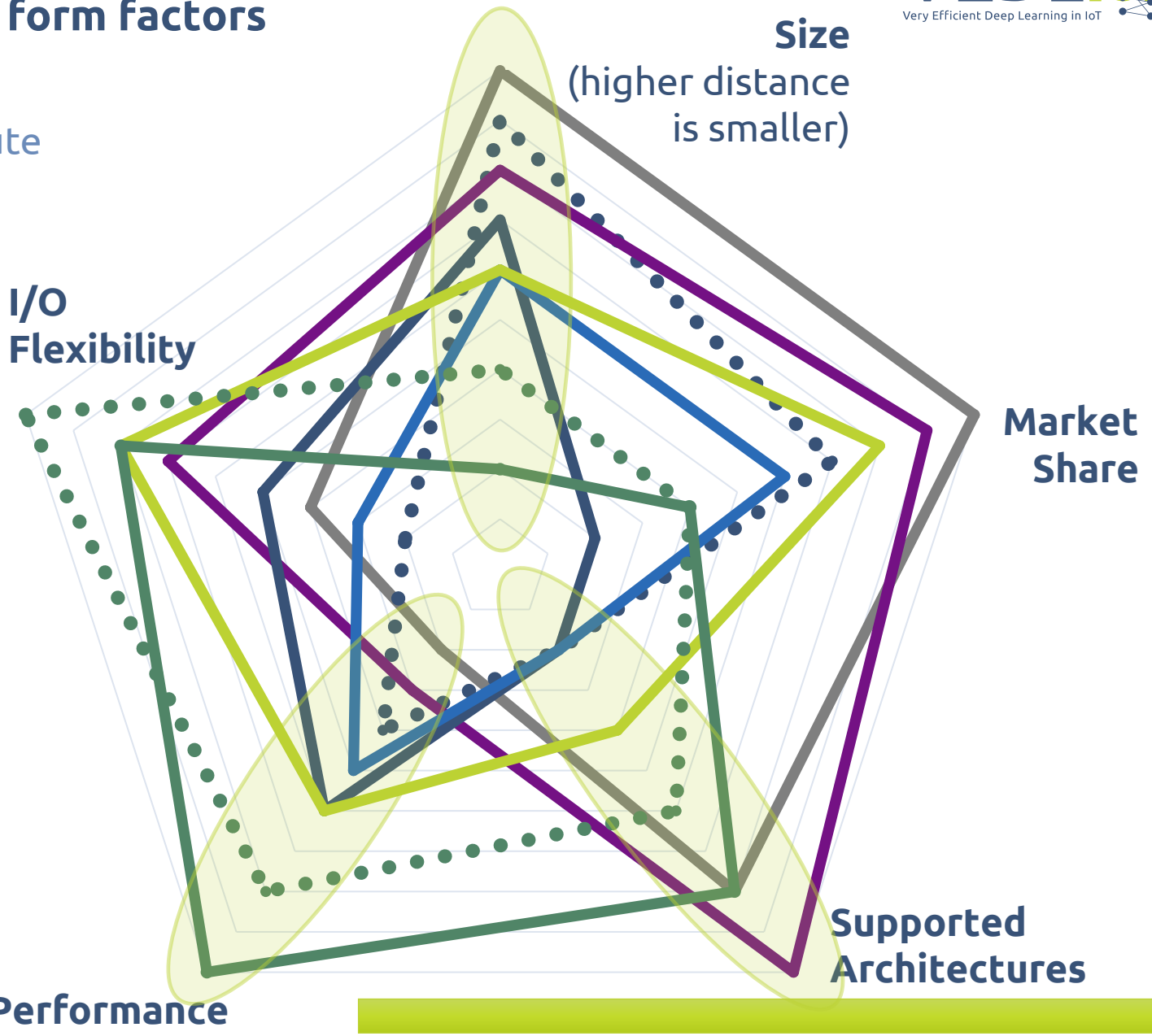
uRECS

RECS|Box & t.RECS

- Raspberry Pi Compute Module 4
- Jetson Xavier NX
- SMARC
- Xilinx Kria
- Jetson AGX Xavier
- COM Express (Type 6/7)
- COM-HPC Client (Type A-C)
- COM-HPC Server (Type D/E)



Flexible and adaptable Accelerators for Deep Learning

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- End of Moore's law & dark silicon
  => Domain Specific Architectures (DSA)
- Efficient, flexible, scalable accelerators for the compute continuum

→ **Algotecture**
- Optimized DL algorithms
- Optimized toolchain
- Optimized computer architecture

Heterogeneous DL Accelerator

DL Model → Compiler → CPU, GPU-SoC, ML-SoC

Algotecture/ Co-Designed DL Accelerator

DL Model ↔ Co-Design → FPGA-SoC

VEDLIoT's Deep Learning Toolchain

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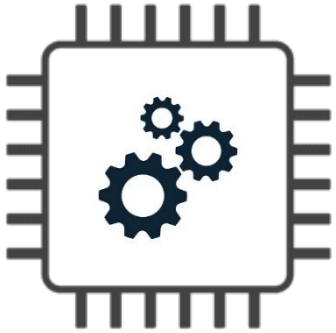
Model Zoo

- Image Classification
- Object Detection
- Semantic Segmentation
- Instance Segmentation
- Extractive Question Answering

Optimization Engine



Compilers & Runtime APIs

tvm

TensorRT

Arm NN

OpenVINO™

Heterogeneous Hardware Platforms

Use case: Smart Mirror – Neural Networks

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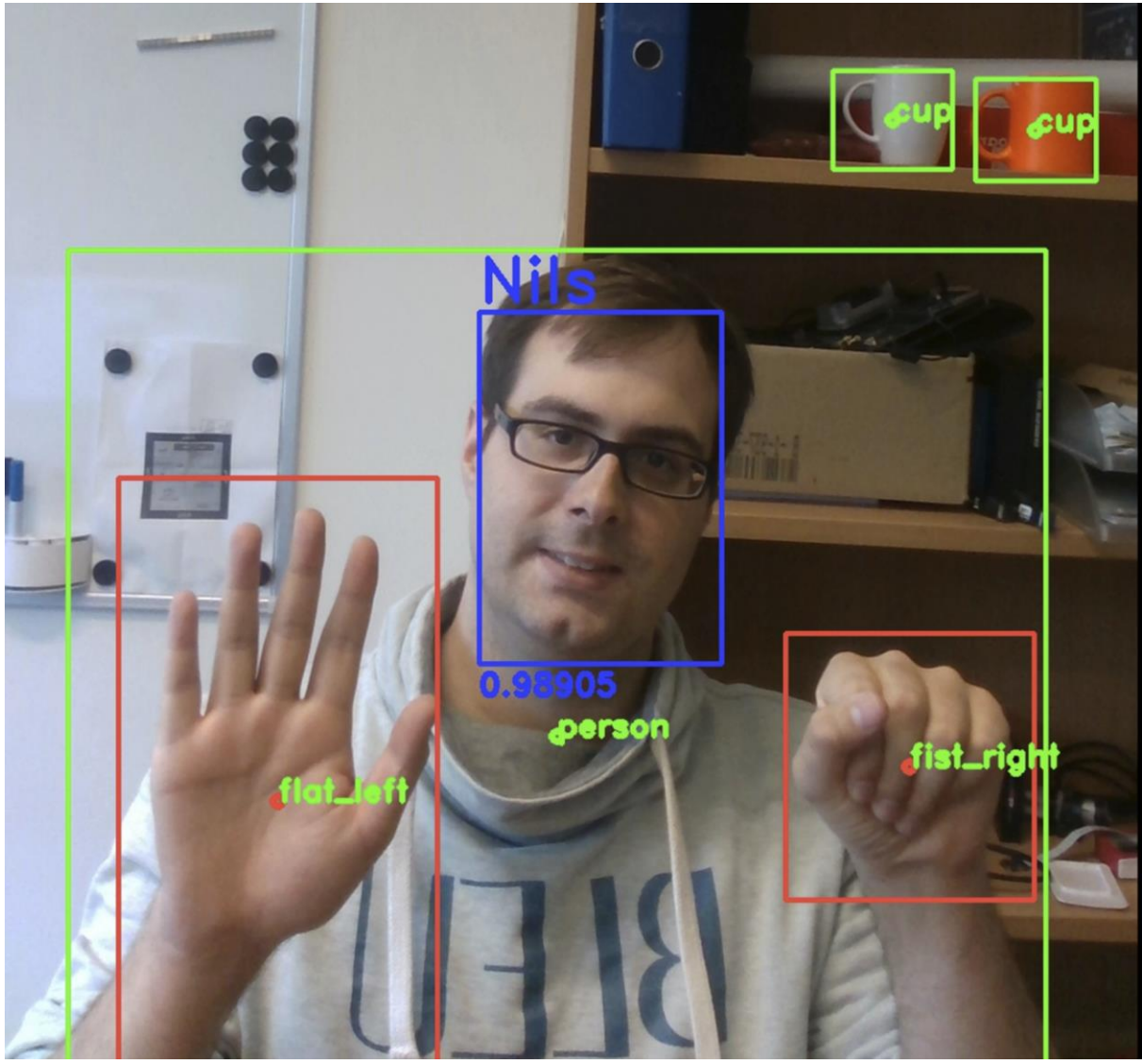
- Face recognition
  - Mobilenet SSD trained on WIDERFACE dataset
- Object detection
  - YoloV3, Efficient-Net, yoloV4-tiny
- Gesture detection
  - YoloV4-tiny with 3 Yolo layers (usually: 2 layers)
- Speech recognition
  - Mozilla DeepSpeech

- AI Art: Style-Gan trained on works of arts

- Collect usage data in situation memory



Use case: Industrial IoT – drive condition classification

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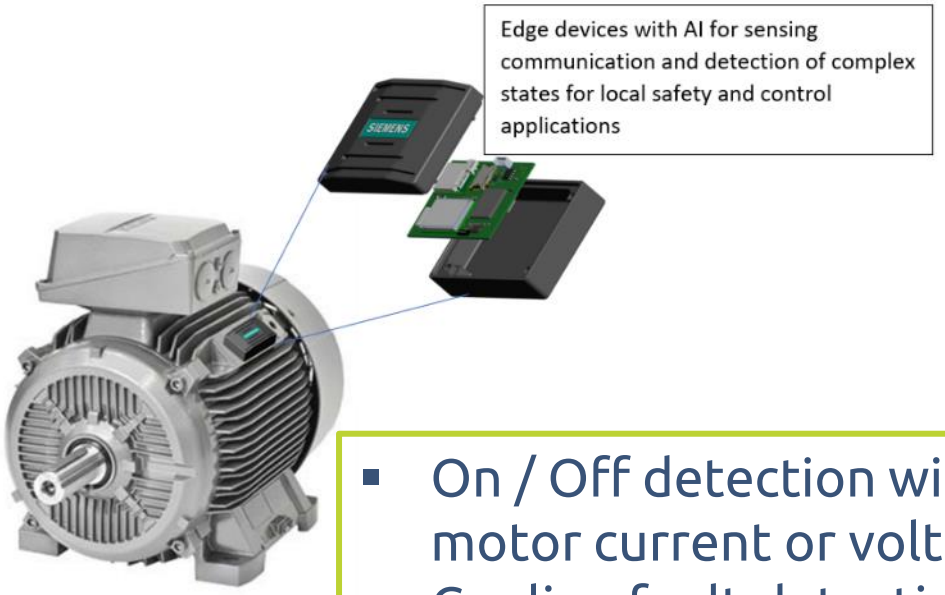
- Control applications need DL-based condition classification
  - On the edge device for low power consumption
  - Suggestions for control and maintenance
- DL methods on all communication layers
  - DL in a distributed architecture
  - Dynamically configured systems
- Sensored testbench with 2 motors
  - Acceleration, Magnetic field, Temperature, IR-Cam (temperature), Current-Sensors, Torque



- On / Off detection without motor current or voltage
- Cooling fault detection
- Bearing fault detection

Use case: Industrial IoT – Arc detection

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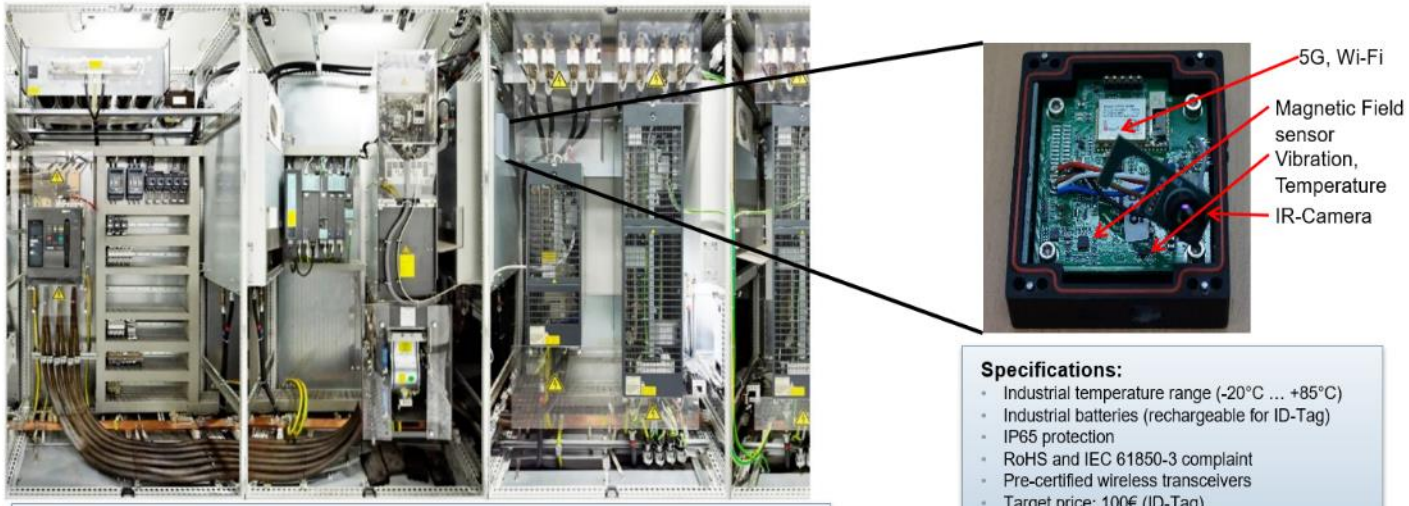
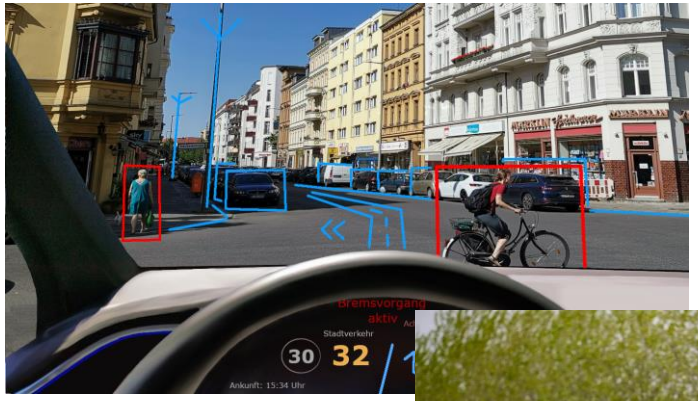
- AI based pattern recognition for different local sensor data
  - current, magnetic field, vibration, temperature, low resolution infrared picture
- Safety critical nature
  - response time should be <10ms
  - AI based or AI supported decision made by the sensor node itself or by a local part of the sensor network

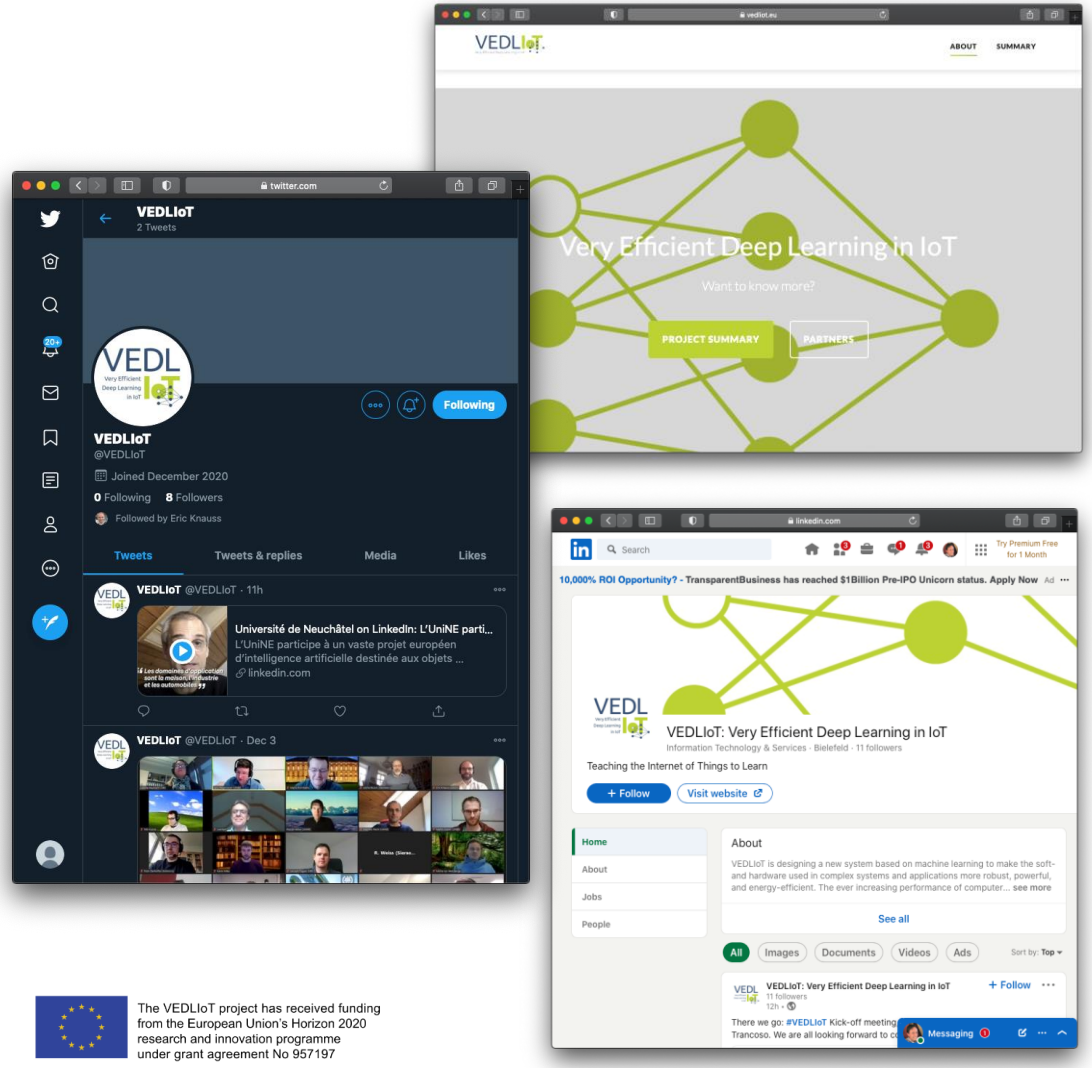


Combining the information from the IR-Camera and the magnetic field sensor to localize electric faults in power cabinets by deep learning methods

Use case: Automotive



- Focus on collision detection/avoidance scenario
- Improve performance/cost ratio – AI processing hardware distributed over the entire chain



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OPEN CALL

Be part of it

⇒ Allow early use and evaluation of VEDLIoT technology

⇒ https://vedliot.eu/use-cases/open-call

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